REMARKS/ARGUMENTS

Claims 1-5, 7, 15-18 and 20-27 are pending in the present application. With this response, claims 1, 3-5, 7, 15-18, 20, 22-25, and 27 have been amended. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 7, 20 and 25 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

The Examiner states:

> **Claims 7, 20, and 25** each recite the limitation "**the** list of occupied end devices" at the end of each claim (emphasis added). There is insufficient antecedent basis for this limitation in the claim.
>
> The Examiner has interpreted the limitation as referring to "**a** list of occupied end devices" (emphasis added).

Office Action dated July 13, 2007, page 3.

Applicants have amended claims 7, 20, and 25 to recite "a list". Therefore the rejection of claims 7, 20 and 25 under 35 U.S.C. 5 112, second paragraph has been overcome and should be withdrawn.

II. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-3, 15-16, 21-22 and 26-27 under 35 U.S.C. § 102(e) as being anticipated by *Zatorski*, System and Method for Controlling Multiple Devices Via General Purpose Input/Output (GPIO) Hardware, U.S. Patent No. 7,069,365, dated June 27, 2006 (hereinafter referred to as "*Zatorski*"). This rejection is respectfully traversed.

The Examiner states:

> **As per claims 1 and 16**, Zatorski teaches a method for performing bus arbitration comprising receiving, by a device driver layer (Figure 3 Item 304) from at least one application included in an application layer (Figure 3 Items 300 and 302, Col 5 Lines 4 - 6), a request to perform a device access operation on an end device on a bus (Col6 Lines 15 - 19), the device driver layer including at least one device driver that communicates with the end device utilizing the bus (Col 6 Lines 26 - 28); determining, by the device driver layer, whether the end device is locked (Col6 Lines 19 - 21, Col 7 Lines 8 - 19); responsive to the end device not being locked, locking, by the device driver layer, the end device (Col6 Lines 21 - 24) and performing the device access

operation (Col 6 Lines 26 - 28); and responsive to the device access operation completing, unlocking the end device (Col 6 Lines 29 - 31).

Office Action dated July 13, 2007, page 4.

Applicants' independent claims recite similar features. Claim 1 is representative of the other independent claims. Claim 1 recites:

"receiving, by a device driver layer from one of a plurality of applications included in an application layer, a request to perform a device access operation on one of a plurality of end devices, the device driver layer including a plurality of device drivers that communicate with the plurality of end devices utilizing a bus;

each one of the plurality of end devices being connected to the bus;

determining, by the device driver layer, whether the one of the plurality of end devices is locked;

responsive to the one of the plurality of end devices not being locked, locking, by the device driver layer, the one of the plurality of end devices and performing the device access operation for the one of the plurality of applications;

responsive to the device access operation completing, unlocking the one of the plurality of end devices; and

another one of the plurality of applications performing a second device access operation to access another one of the plurality of end devices while the device access operation is being performed, wherein the bus is not locked while the device access operation is being performed and the one of the plurality of end devices is locked."

Zatorski does not anticipate Applicants' independent claims because *Zatorski* does not teach receiving, by a device driver layer from one of a plurality of applications included in an application layer, a request to perform a device access operation on one of a plurality of end devices, the device driver layer including a plurality of device drivers that communicate with the plurality of end devices utilizing a bus.

Zatorski teaches a south bridge 114 that includes a shared register 200. The south bridge is coupled to both a PCI bus 110 and an ISA bus 120. The south bridge is coupled to a device 116 and a device 118 using pins 204. Devices 116 and 118 share shared register 200. A nexus device driver 304 arbitrates between device 116 and device 118 for access to shared register 200.

The nexus device driver 304, device drivers 300 and 302, and a root device driver 306 are included in software 124. The software 124 is included in memory 104, which is coupled to system bus 106.

The Examiner asserts that the nexus device driver 304 of *Zatorski* is analogous to the "device driver layer" claimed by Applicants. Applicants' independent claims describe the device driver layer

including a plurality of device drivers. The nexus device driver 304 does not include a plurality of device drivers. Therefore, the nexus device driver 304 is not analogous to the "device driver layer", and *Zatorski* does not anticipate Applicants' claims.

Applicants' claims also recite: "each one of the plurality of end devices being connected to the bus". *Zatorski* also does not anticipate Applicants' independent claims because *Zatorski* does not teach "each one of the plurality of end devices being connected to the bus".

It appears the Examiner is asserting that the shared register 200 is analogous to an end device. The Examiner asserts that *Zatorski*, column 6, lines 15-19, teaches "a request to perform a device access operation on an end device on a bus". This section of *Zatorski* is reproduced below:

> When one of the device drivers 300 and 302 generates an access request directed to the shared register 200 (e.g., including the address of the shared register 200), the nexus device driver 304 receives the access request.

Zatorski, column 6, lines 15- 19.

Applicants disagree that the shared register is analogous to an end device because the shared register 200 is not connected to a bus. The shared register 200 is included within south bridge 114. While south bridge 114 is connected to PCI bus 110 and ISA bus 120, *Zatorski* does not teach the shared register being connected to PCI bus 110, ISA bus 120, or any other bus.

Furthermore, the shared register is not analogous to an end device because Applicants claim a plurality of end devices. *Zatorski* teaches only one shared register.

The Examiner also asserts that *Zatorski*, column 6, lines 26-28, teaches "the device driver layer including at least one device driver that communicates with the end device utilizing the bus". Applicants disagree. This section of *Zatorski* is reproduced below.

> Following the obtaining of the software lock, the nexus device driver 304 may access the shared register 200 for the device driver.

Zatorski, column 6, lines 26-28.

Nothing in this section of *Zatorski* teaches a bus. Therefore, this section of *Zatorski* does not teach an end device connected to a bus.

Because *Zatorski* does not teach "each one of the plurality of end devices being connected to the bus", *Zatorski* does not anticipate Applicants' claims.

Applicants' claims also recite: "determining, by the device driver layer, whether the one of the plurality of end devices is locked". *Zatorski* also does not anticipate Applicants' claims because *Zatorski* does not teach this feature.

The Examiner asserts that *Zatorski*, column 6, lines 19-21, and column 7, lines 8-19, teaches "determining, by the device driver layer, whether the end device is locked". These sections are reproduced below.

> If the nexus device driver 304 determines the request is valid (as described below), the nexus device driver 304 may initiate a "locking" procedure during which the nexus device driver 3 04 obtains a software "lock" permitting exclusive access to the shared register 200.

Zatorski, column 6, lines 29-24.

> During the operation 404, the ownership bits of the device driver initiating the register access are checked. A determination is made as to whether the register access is "valid" during the decision operation 406. For example, a read access to the shared register may always be judged valid. For a write access to the s h d register, the shared register may be read, and the contents of the shared register may be compared to write data of the register access. The memory location containing the ownership bits of the device driver initiating the register access may also be read. The register access may be judged valid if the write data will change only bit positions of the shared register owned by the device driver initiating the register access.

Zatorski, column 7, lines 7-20.

It appears the Examiner is asserting that the nexus device driver 304 obtaining a software lock is analogous to "determining by the device driver layer, whether the one of the plurality of end devices is locked". Applicants disagree.

Zatorski teaches the nexus device driver 304 obtaining a software lock, which permits exclusive access to the shared register 200. As discussed above, the nexus device driver 304 is not described as including a plurality of device drivers, and, therefore, cannot be analogous to a device driver layer that includes a plurality of device drivers. Furthermore, the shared register is not analogous to one of the end devices because the shared register is not connected to a bus. Therefore, the nexus device driver 304 obtaining a software lock does not teach, "determining, by the device driver layer, whether the one of the plurality of end devices is locked".

Applicants also claim "responsive to the one of the plurality of end devices not being locked, locking, by the device driver layer, the one of the plurality of end devices and performing the device access operation for the one of the plurality of applications; responsive to the device access operation completing, unlocking the end device". As discussed above, *Zatorski* does not teach a device driver layer or end devices as claimed by Applicants. Therefore, *Zatorski* does not anticipate Applicants' claims because *Zatorski* does not teach these features.

Applicants also claim "another one of the plurality of applications performing a second device access operation to access another one of the plurality of end devices while the device access operation is being performed, wherein the bus is not locked while the device access operation is being performed and the one of the plurality of end devices is locked". *Zatorski* does not anticipate Applicants' claims because *Zatorski* does not teach these features.

For the reasons given above, *Zatorski* does not anticipate Applicants' claims.

In addition to the features discussed above, independent claim 15 further limits the bus to being an Inter-Integrated Circuit (IIC) bus. Claim 15 also further describes the plurality of end devices being attached directly to the bus. *Zatorski* does not teach either one of these features. Therefore, because *Zatorski* does not teach these features and for the reasons given above, *Zatorski* does not render claim 15 obvious.

Applicants' claims 2, 21, and 26 describe the device access operation being one of a read operation and a write operation. *Zatorski* does not anticipate these claims because *Zatorski* does not teach a device driver layer, which includes a plurality of device drivers, receiving a request to perform a device access operation that is one of a read operation and a write operation.

Applicants' claims 3, 22, and 27 describe responsive to the one of the plurality of end devices being locked, denying the device access operation. *Zatorski* does not anticipate these claims because *Zatorski* does teach a plurality of end devices.

All remaining claims depend from one of the independent claims discussed above and are patentable for the reasons given above.

Therefore, this rejection has been overcome and should be withdrawn.

III. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 4-5, 7, 17-18, 20, and 23-25 under 35 U.S.C. § 103(a) as being unpatentable over *Zatorski* in view of *Freitas* et al., Method for Managing Concurrent Processes Using Dual Locking, U.S. Patent No. 6,401,110, dated June 4, 2002 (hereinafter referred to as "*Freitas*"). This rejection is respectfully traversed.

Applicants' claims 4-5 and 7 are representative of claims 17-18, 20, and 23-25.

Claim 4 recites: "wherein the step of determining whether the one of the plurality of end devices is locked includes determining whether an address of the one of the plurality of end devices is found in a list of occupied ones of the plurality of end devices, wherein the plurality of end devices are separate and distinct and distinct end devices".

Claim 5 recites: "wherein the step of locking the one of the plurality of end devices includes placing a device address of the one of the plurality of end devices in a list of occupied ones of the plurality of end devices, wherein the plurality of end devices are separate end devices".

Claim 7 recites: "wherein the step of unlocking the one of the plurality of end devices includes removing the device address from the list of occupied ones of the plurality of end devices".

The Examiner states that *Zatorski* does not teach the features of these claims and relies on *Freitas* to cure the deficiencies of *Zatorski*. Applicants disagree that *Freitas* cures the deficiencies of *Zatorski*.

Freitas teaches each processor maintaining a lock table with multiple entries. Each entry corresponds to a subpart of a shared resource. In contradistinction, Applicants' claims describe a list of occupied ones of the plurality of end devices, wherein the plurality of end devices are separate and distinct end devices. A subpart of a shared resource is not analogous to one of a plurality of end devices that are separate and distinct end devices. Thus, *Freitas* does not cure the deficiencies of *Zatorski*. Therefore, the combination of *Zatorski* and *Freitas* does not render Applicants' claims obvious.

Therefore, the rejection of claims 4-5, 7, 17-18, 20, and 23-25 under 35 U.S.C. § 103(a) has been overcome and should be withdrawn.

IV. Conclusion

It is respectfully urged that the subject application is patentable over the cited prior art and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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